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Reliability and Availability Considerations about Electronic Train Detection System

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ABSTRACT

This paper presents some considerations about the reliability and availability evaluation of a Trains Detection System designed using axle counter method and implemented with redundant distributed microprocessor architecture.

The System was designed using modern and structured design methodology for software and hardware which provides better degrees of reliability with low money expenses.

The System architecture and design methodology furnished estimated failure rates of 52.475 x 10E-6 per hour or a MTTF (Mean Time To Fail) of 2.2 years for each counting point and a availability of five nines. By the way was obtained a MTBUF (Mean Time Between Unsafe Failures) of 69 years.

The paper presents a brief description of the system hardware architecture, showing the modules and elements, specially the axle counter. Following the Reliability and Availability of all system is discussed comparing the degrees obtained for the system.

INTRODUCTION

This paper presents the estimation method for the Reliability and Availability Index for the Electronic Train Detection System (DET) developed at Digital Systems Laboratory of Escola Politécnica da Universidade de São Paulo, through Foundation for

The project had been sponsored by CMSP (São Paulo Metropolitan Subway Company) to be installed at Itaquera Train Yard where the new equipment would be homologated.

In the next sections it will be described the parts of DET and the process used for estimation of its Reliability and Availability marks.

BRIEF DESCRIPTION OF THE DET

DET implements the first level of data aquisition for the signalling system, that assures reliability for the railway. With the status informations of the "track circuits" (train detection) the Trains Movement Controler (CMT) makes the route interlocking to the safe trains movement in the yard.

DET uses the axle counter method. The axle counter is a very usual method in many countries, but there are no informations of its commercial use, in such application, in Brazil. The operation principle is: count the number of axles in a track section delimited by axles sensors, subtract the number of outgoing axles and add the number of incoming ones. This method uses puntual sensors in a continuous signalized sector. The basic system is presented in figure 1.

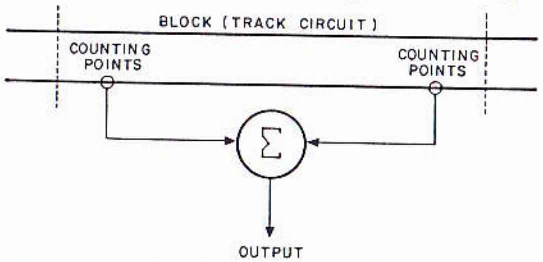


Figure 1 - Axle counter basic schema

DET is implemented by a number of wheels sensors and by a computing equipment (of the number of axles in each sector). The sensors are implemented with infra-red light technology, designed with fail-safe philosophy, and the axle counter is implemented by a number of microprocessor boards interconnected in a triplicated computing array. The fail-safe design and the compared redundancy adds an appropriate reliability and availability to the system, as will be evaluated in this paper.The great number of sectors needed for convenient yard departu[illegible] operations lets to its division in blocks. Each bl[illegible] receives a axle counter equipment.

Each axle counter equipment is responsible for the supervision of 64 counting points. This division makes easy the implementation of the axle counters and minimizes the cable needs [1] [2] [3].

The electronic interlocking, that receives the information about the occupation of each track-circuit, is triplicated and works in the compared redundancy, with the accordance of, at least, two of the three processors systems. The control actions takes place after the vital voting [4].

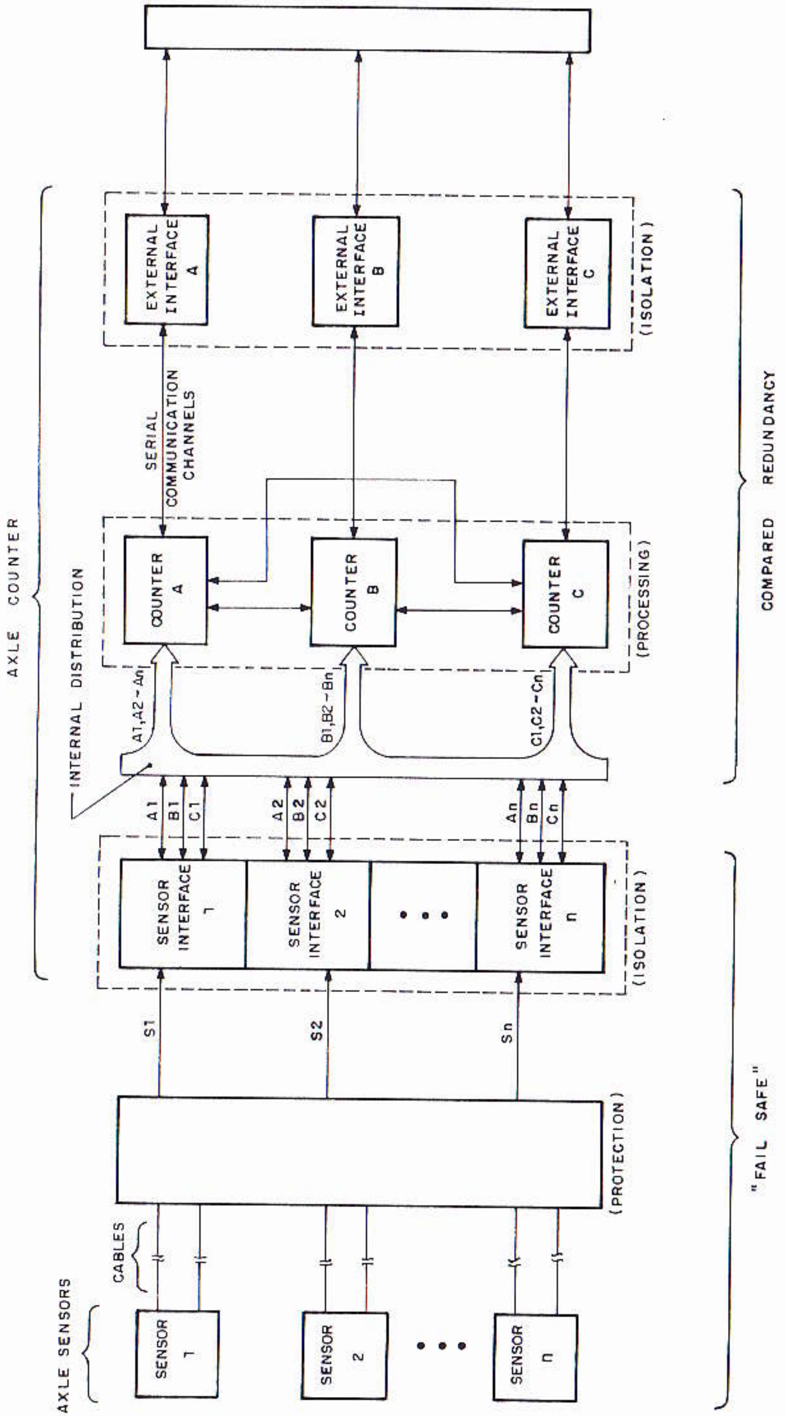
The axle counters are triplicated allowing a simple interconnection scheme, with each channel of the counter (interlocking processor system) interconnected to each wheel sensor. The security of the detection is also assured by the vital votation to generate the outputs. There exists an internal votation in the DET, that performs the auto-diagnosis functions. A block diagram of the DET may be observed at figure 2.

AXLE COUNTER

The historical development efforts of the axle counters induces some choices about the technological aspects of a new development in this area. The way of the evolution, from the electromechanical counters [5], passing through the logic gates and fail-safe memories [6], to the digital gates with TTL technology associated with a functional supervisor for better reliability [7], and the natural increasing of digital circuits integration, the auto-test, the diagnosis and the software votation technics, leads to microprocessors systems.

The axle counter of the DET system was developed and implemented with digital technology, considering its simplicity and low costs without compromising its reliability level.

The axle counter analyses the signals generated by the sensors and performs the characterization of the wheel passage, determining the direction of the movement, counting the axles in a block, and determining the occupation state of the block. This is a simple job when the implementation of the system is made by microprocessors in a convenient architecture.



The reliability characteristics are based on compared redundancy, where two or more elements do the same job in an independent way, and each result is compared and voted. In case of doubt, the system provides the safe state. The compared redundancy is the most adequate solution, because it permits the use of microprocessors in reliable systems, considering that microprocessors themselves are not enough reliable.

The counter function is executed by an equipment implemented by a chain of microprocessors, operating in a parallel mode. The architecture was especially developed for this application. The information about the state of each block is sent to the higher level systems, like the Centralized Traffic Control System and the Interlocking System, by serial communication channels.

The performance and the flexibility of the counter system are provided by its multiprocessors architecture, that permits till sixteen microprocessor boards working in parallel, with communication between them provided by internal serial channels. The architecture of the counter system permits the combination of configurations, with redundant elements and functions, that become manifest in the improvement of the availability and reliability on all system.

The axle counter module (MCX) is implemented by a group of printed circuit boards of digital processors, interconnected by a bi-directional multipoint internal serial channel. This arrangement characterizes the MCX as a multiprocessor system, where each processor executes distinctive work and may cooperate with other processor by the communication channel. This characteristic allows a distribution of the entire job in a number of processors working together, and new works can be made by the allocation of new jobs in the microprocessors of the array, without degradation at the system performance.

RELIABILITY OF THE COUNTER SYSTEM

In this item the reliability and availability indexes of the DET system are evaluated.

The designers had evaluated the reliability index of each element, to get better design decisions. This indexes can not be considered in a formal reliability analysts. These dependency may carry all the polarizations that could be present in the conception design, but it is useful and necessary as a way to evaluate the goals. The references [8] [9] made equivalent analysis.

All the indexes were obtained by the component counting method, all the failure rates was gotten from the MIL-HDBK-217-D of the Defense Department of the United States [10]. The ambient was defined as "Ground-mobile", Gm, that means severe conditions. The obtained failure rates are listed in table 1.

TIV	3,86472	10E-6/h	72.126 h
RIV	8,21842	10E-6/h	35.438 h
PRS	0,19242	10E-6/h	98.112 h
IRS(sensor side)	0,2	10E-6/h	5 E+6 h
IRS(count.side)	6,20837	10E-6/h	161.07 h
PP	26,99255	10E-6/h	37.047 h
PM	49,18040	10E-6/h	20.333 h
ISO	17,61816	10E-6/h	56.760 h
FCM	36,54126	10E-6/h	27.366 h

TIV - Optical Transmitter
RIV - Optical Receiver
PRS - Voltage pre-regulator of the sensor
IRS - Isolation interface
PP - Parallel processor
PM - Serial processor
ISO - Isolation interface
FCM - Power supply for the counter

Table 1 - Failure rates of the PCBs

The failure rate of each counting point may be obtained by the adequate summation of the failure rates of its components. In that way, a group of one TIV, one RIV, one PRS and the part of an IRS (the side of the sensor) have an estimated failure rate of 52.47556x10E-6 /h, or a MTTF of 19,056.49 hours, that means 2.2 years.

Considering that, when the counting point is in fail, the maintenance team can join the boundary blocks together leading to another bigger one, and that always exists a maintenance team available in the yard, any maintenance may be done in two hours, what furnishes a repair rate of 0.5. This maintenance is

maintenance is needed, because in this case all information stored in the system memories is loosed and it is necessary restart all blocks with its occupancy status; for this the repair rate is taken to be 0.25 or four hours of work, it is important note that this kind of failure is extremely improbable.

By Markov modeling (born and death [11] [12] [13] with a MTTF (Mean Time to Fail) and a MTTR (Mean Time to Repair) given by the inverses of the failure and repair rates, respectively), the availability (A) would be given by:

$$A = \frac{MTTF}{MTTF + MTTR}$$

This furnishes A = 0.9998, or two hours out of order for each 10.000 hours (1.6 years) of work.

With the numbers of table 1 is easy to find the rates for the axle counter system. One channel of the redundant module has a failure rate that is the summation of the failures rates of each one of its parts, i.e., eight PP boards, two PM boards, one ISO board, one FCM board and one channel of one IRS board. The failure rate of the axle counter system is 364,669x10E-6/h (2.669 hours).

Using the Markov modeling one can find an availability (A) of 0.999993 (five nines). This means seven hours of unavailability for a million hours of work (116 years). This is a good result for a initial system specification of four nines.

The initial MTBUF (Mean Time Between Unsafe Failure) specification (greater than 100,000 years) is difficult to be directly verified. A pessimist trial would be possible if considering unsafe all the time that the system is with two channels out of order like the state two in figure 4, what is not totally true, but it is hypothesis. With this hypothesis, with a modeling like a used in [14] one may say that the medium time interval that the system stay in any state m_{ii} is given by:

$$m_{ii} = \frac{\text{medium time in state } i}{P\ (\text{being in } i\text{, for finite time } t)}$$

Considering state 2 as an unsafe state, one may

$$m_{22} = \frac{1}{\mu_2 * P2}$$

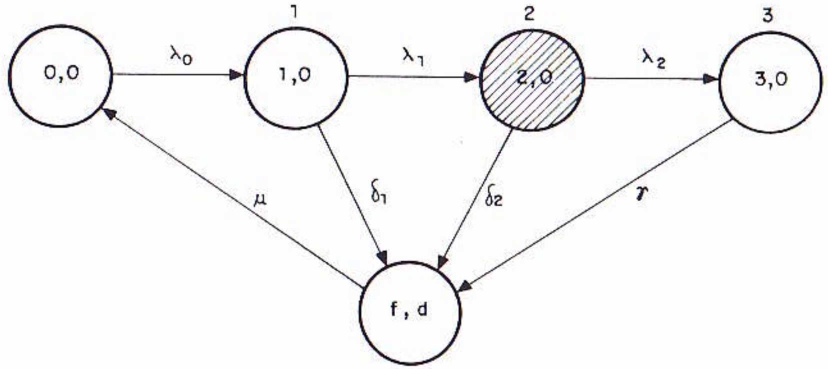
getting 594,880 hours (69 years) as result. This number do not fit the specified 100,000 years.

In order to get more detailed analysis, it is necessary consider the software reliability functions, which have been neglected until now. A very important function performed by software is the verification of the correct functioning of the involved hardware. This is a auto-diagnoses function that isolates the processor in case of doubt about its integrity. This function analyses all message exchange verifying the correct functioning of the processors. Any doubt about the integrity of any processing channel inhibit the answers. This failure detection system assures the veracity of information at the system's output.

With this reliability function implemented by software, the repair rate in the formula is substituted by the failure detection rate. The system would have unsafe outputs only while the software doesn't detect the failure; during the time between the detection and the repair the system is safe. The model that considers this situation can be seen in figure 3.

If a one second failure rate detection is considered, a very reasonable number is 4,34x10E+9 hours (the M22 may be calculated as in the previous case), or 495,000 years, exceeding the original specification.

Its important to note that, in all these calculations, the software is considered to be perfect, i.e., the software reliability itself was not taken into account. For that this restriction could be released it would be necessary an equivalent analysis in the software, the references [15] [16] [17] [18] [19] and [20] analyses this problem.



(f,d) NUMBER OF FAILURES, NUMBER OF DETECTED FAILURES

$f \neq 0$: ANY > 1

$d \neq 0$: ANY > 1

δ_1 = DETECTION RATE WITH ONE FAILED UNIT (MTTD = 1 sec)

δ_2 = DETECTION RATE WITH TWO FAILED UNIT (MTTD = 2 sec)

γ = DETECTION RATE WITH THREE FAILED UNIT (MTTD = 3 sec)

γ = DETECTION BY EXTERNAL ELEMENT (e.g. CMT)

μ = REPAIR RATE

λ = FAILURE RATE OF ONE UNIT

$\lambda_0 = 3\lambda$

$\lambda_1 = 2\lambda$

$\lambda_2 = \lambda$

$\mu = 0,5$

$\lambda = 374,7 \cdot 10^{-6}$ f/h

$\delta_1 = 3600$ d/h

$\delta_2 = 1800$ d/h

$\gamma = 1200$ d/h

$$P_2 = 1,28 \cdot 10^{-13}$$

$$m_{22} = \frac{1}{P_2\,(\lambda_2 + \delta_2)}$$

Figure 3- Markov's model with software detection

CONCLUSIONS ABOUT THE QUALITY LEVELS

The initial challenge, the implementation of a system with four nines of availability, had been reached with advantages. The five nines is the result of the triplication of the counter and the high reliability achieved in the field equipment [21].

This results suggests that the triplication was not needed in a departure yard, but the index are important to let the system be homologated for use in a commercial line application.

It is very dificult to compare the results obtained with the indexes of other systems, because there are no normalization or any consensus about them [15].

The international tendency of microprocessors utilization in the implementation of reliable functions takes time to get the railway systems, because the cost competitivety and the incredibility of designers in the new digital technology.

The DET have been submitted to field tests with good results. The tests had taken place at Itaquera Departure Yard, in a region of maximum dust and vibration (line of break tests).

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Object Oriented Constraint Representation for Railway Traffic Optimisation

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ABSTRACT

Railway Traffic Management is basically a constraint satisfaction problem.
Optimisation problems are traditionally approached by the operation research. Constraint programming is a more recent approach.
We propose an innovative approach, based on expert system technology, which is centered on the representation of the constraints that the Railway network has to satisfy and on the management of such constraints.
Object Oriented paradigm is very natural and intuitive in knowledge representation and Object Oriented programming is very efficient. In particular Object Orientation looks very suitable and promising for constraint representation.
This paper will explain why railway traffic management is concerned with constraint representation problem, how this approach has been applied to railway traffic optimisation, allowing the implementation of the PORT (Planning for Optimisation in Railway Traffic) Expert System.

RAILWAY TRAFFIC MANAGEMENT SYSTEM

Railway Traffic Management Problems and Automatic Supervision Systems

The continuing evolution in Information Technology is taking place in centralized control system for railways and rapid transit networks.
Modern railway traffic management systems are usually highly

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